# Board 2 Report

555 Timer/Hex Inverter Circuit with and without Ground Plane

ECEN5730 Fall 2025

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# Project Overview

## Plan of Record (POR)

- Create Schematic for Inverter Circuit **(Complete Week 5)**
- Test the schematic/hex inverter on solderless breadboard (with BOM, selected by the class) **(Completed Week 5)**
- Add PCB design of Inverter circuit by reducing extraneous parts on Board 1 and updating indicator lights, testpoints, and jumpers **(Completed Week 6)**
- Do CDR of PCB Design **(Completed Week 6 with TA)**
- Bring-up PCB Board 1 for 555 Timer (only) to test the timer post-assembly **(Completed Monday of Week 7)**
- Bring-up PCB Board 2 (with Hex Inverters) after assembly and record/compare measurements for inverters with and without ground plane **(Completed Week 10)**

## Project Goals (Working Board)

- Take advantage of existing circuit from Board 1 to reduce risks
- Indicator LEDs are properly placed and lights up for both inverters and power rails
- Noticeably lower voltage spikes/drops on Inverter with a ground plane compared to one without a ground plane
- Circuit is easily debuggable, with accessible test points to measure power rail noise during transition for both inverters
- Both inverters are able to power on from either 5V (power jack) or 3.3V (LDO)
- No issues with board assembly
- Be on Schedule

## Sketch of the Schematic

*555 Timer, From Board 1*

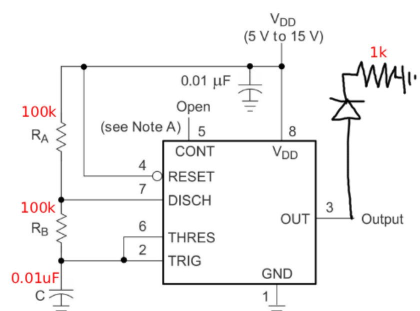


Figure 1: 555 Timer Circuit

This design creates a circuit with 480Hz, 66.6% duty cycle timer. Initial capacitor sizes are small at 0.01uF. This schematic was tested in a solderless breadboard, which resulted in a circuit with similar frequency and duty cycle.

*Hex Inverter*

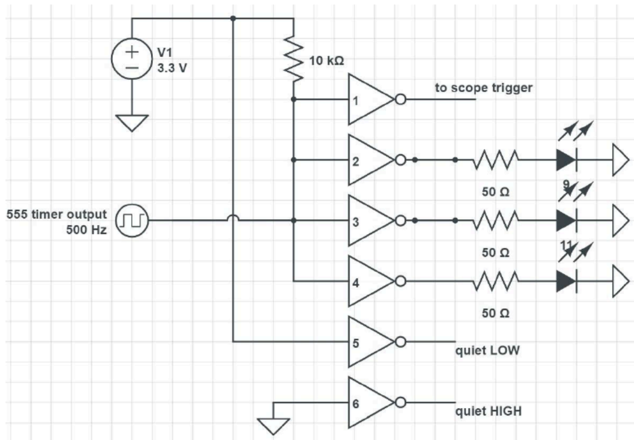


Figure 2: Hex Inverter Circuit

Output of 555 Timer is not connected to inputs of Hex inverter (powered by 3.3V LDO output, with a 10k pull up resistor). VCC and GND are connected to 2 of hex inverter input pins to measure quiet LOW and quiet HIGH noise. LED pins are connected to output after a 50 ohm resistor. Outputs of the inverter were verified on a solderless breadboard.

*Low-Dropout (LDO) for Power Select*

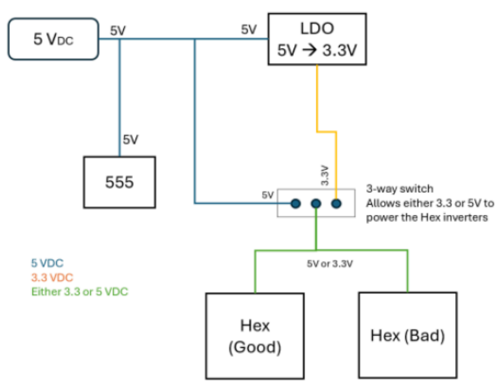


Figure 3: Power Rails for Board 2

A 3-pin jumper will be used to select either 5V or 3.3V power as seen in the power tree above.

## Altium Designer Schematic

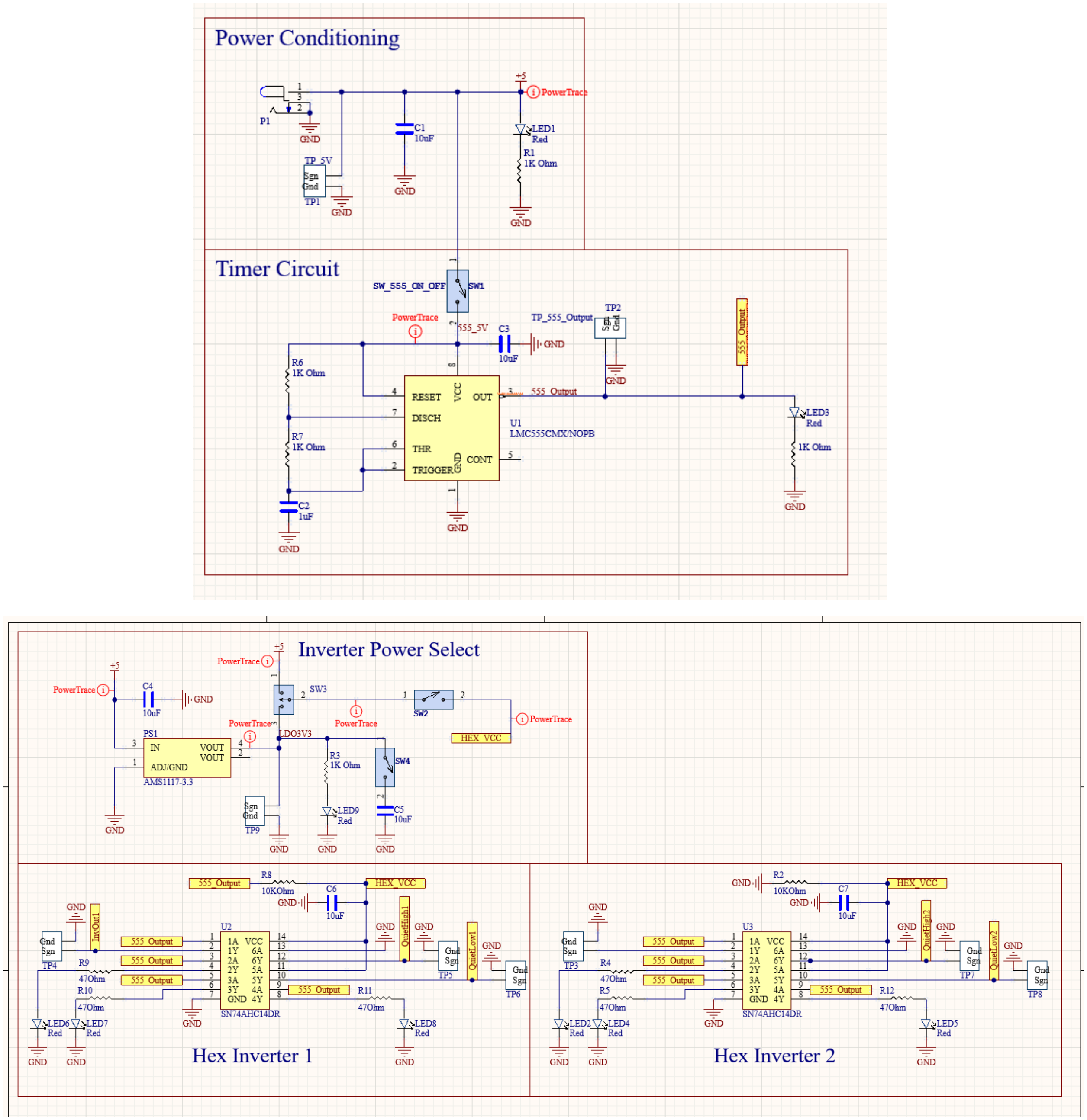


Figure 4: Altium Schematic for Board 2 (Top: 555 Circuit, Bottom: Hex Inverter Circuit)

Existing designs of 555 Timer Circuit (Board 1) were stripped down to only include basic indicator lights and test points. 3.3V LDO (ams1117-3.3) output is connected to a 3-pin jumper (for 5V/3.3V power select) to provide alternative VCC for both hex inverters (SN74AHC14DR).

Output for 555 Timer is pulled up with a 10k resistor, and each hex inverter uses all 6 input pins, 3 of which are used to drive LEDs, 1 for Test Point, and 1 each for quiet HIGH and LOW. Circuit for Hex Inverter 1 and Hex Inverter 2 are identical on schematic. Test points were added to monitor noise on the hex inverter output, quiet HIGH, and quiet LOW.

## PCB Board Layout

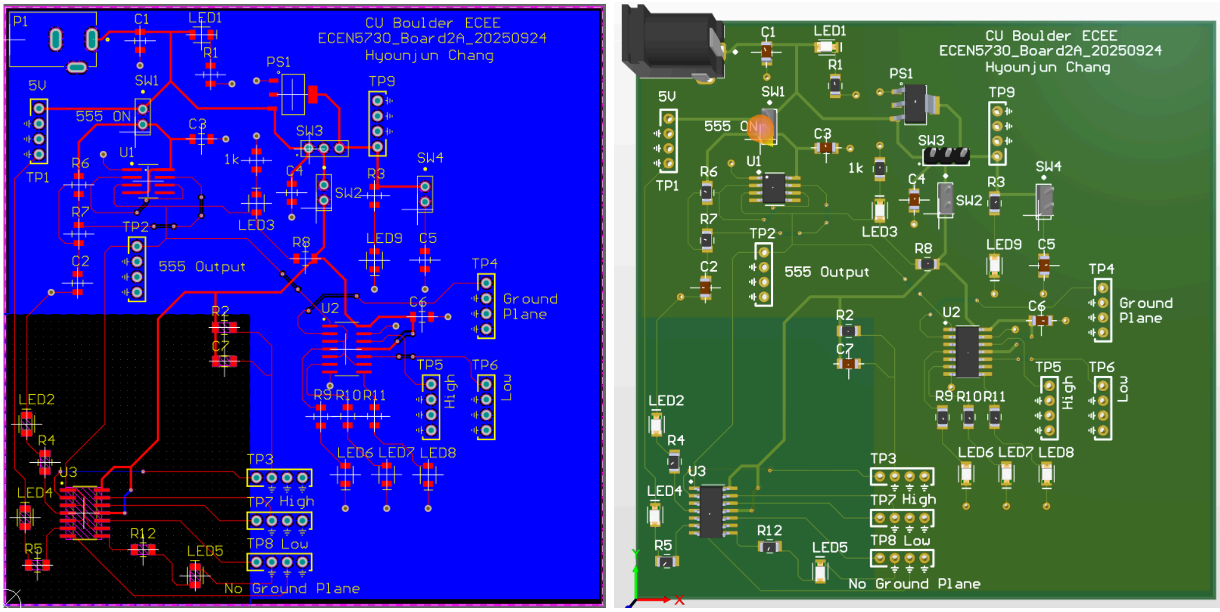


Figure 5: PCB Design on Altium Designer 2D view (Left), 3D view (right)

Area without the blue plane the area on the PCB without Ground Plane. One hex inverter is placed on plane w/o ground plane, with decoupling capacitors placed far away with long traces. The other hex inverter is on the ground plane, with decoupling capacitors placed nearby.

## Picture of Physical Board

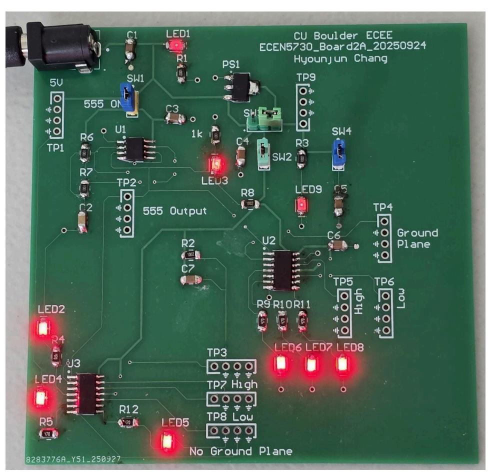


Figure 6: Assembled Board 2 with Indicator Lights of Hex Inverter operating at 3.3V

# Board Functionality:

Test Points:
TP1: 5V Power Rail Test Point
TP2: 555 Circuit Test Point
TP9: 3.3V LDO Test Point
TP3: No Plane Inverter Test Point
TP7: No Plane Quiet High Test Point
TP8: No Plane Quiet Low Test Point
TP4: Ground Plane Inverter Test Point
TP5: Ground Plane Quiet High Test Point
TP6: Ground Plane Quiet Low Test Point

## Expected Working Board:

- Stable 5V power-rail output on TP1, and 3.3V output on TP2, with LED indicators (LED1 and LED9 respectively) turning on.
- TP2 outputs a 480Hz 67% duty cycle clock, with same Vpp (5V), when SW1 connected
- LED2,4,5 (no plane), and LED 6,7,8 (ground plane) light up when SW2 connected
- TP3 (no plane) and TP4 (ground plane) have similar high voltage as input (555 circuit)
- Much higher Quiet Low/High bounce on no plane (TP7, 8) compared to ground plane (TP5,6)
- Higher rail collapse on inverter without ground plane due to return path

## Actual Assembled Board:

Oscilloscope probe and spring connector (for ground) was used to measure signals for all test points to minimize noise. 555 Circuit from Board 1 is working as expected, outputting 505Hz signal with 67% duty cycle.

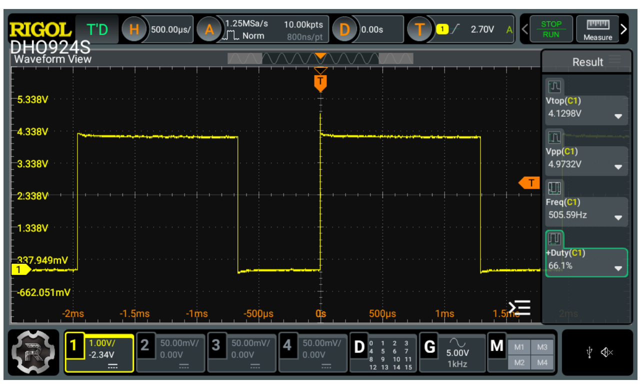

Figure 7: Output from 555 timer module without load

Inverter Vcc of 3.3V was used. The noise level of the inverter without ground plane and far decoupling capacitor was lower than the one with ground plane, which was surprising. This is due to the fall time of the 555 signal due to inductance of further decoupling capacitors as seen below.


Figure 8: Rising Edge of Inverter (Left: No ground plane, Right: Ground Plane), 1V scale

However, noise in the Quiet Low/Quiet high tells a different story: noise of inverter without ground plane is much higher by more than factor of 5, due to return path being much longer (higher inductances).

| Inverter Vcc=3.3V | Quiet High | Quiet Low |
|---|---|---|
| No Ground Plane | 2.66Vpp | 10.64Vpp |
| Ground Plane | 0.43Vpp | 1.86Vpp |

Figure 9: Quiet Low/Quiet High Noises on Board 2 for Vcc = 3.3V


Figure 10: Quiet High/Low Noise during 555 Posedge (Left: No ground plane, 2V scale, Right: ground plane, 500mV scale)

Rail compression, calculated by the difference of Quiet High and Quiet low is more evident without a ground plane. The voltage difference between Vcc and Gnd falls to ~2V for the inverter without a ground plane, compared to ~2.6V with the ground plane. However, the overshoot of rail compression was higher on the inverter on the ground plane due to faster rise time of 555 input.

| Inverter Vcc=3.3V | Rail Vcc_low | Rail Vpp |
|---|---|---|
| No Ground Plane | ~2.0V | 1.6V |
| Ground Plane | ~2.6V | 1.3V |

Figure 11: Rail Compression (Quiet High Voltage - Quiet Low Voltage) for Vcc = 3.3V

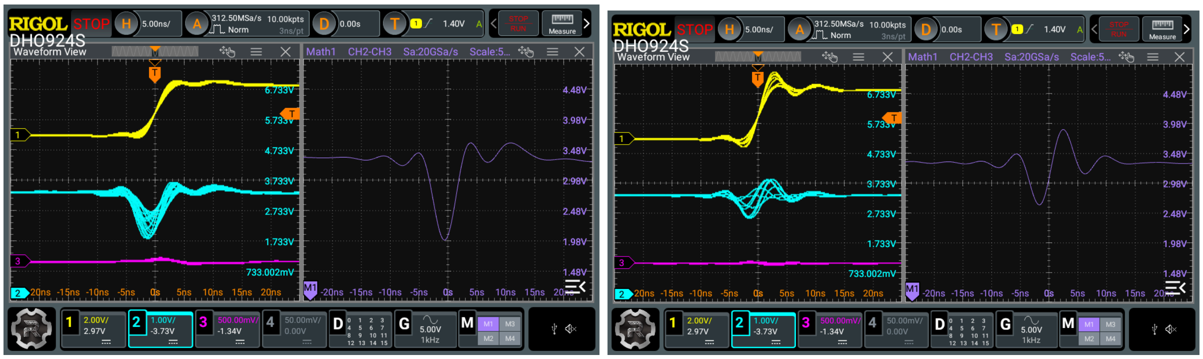


Figure 12: Rail Compression during 555 Posedge (Left: No ground plane, Right: ground plane)

## Conclusion:

When designing a PCB, ground plane and decoupling capacitor plays a huge role, and decoupling capacitors must be placed close to Vcc of a part to minimize rail compression. Long traces/wires are more susceptible to noise due to inductance. Ground planes allow the return path to be much shorter, since you connect to a ground nearby through a via.

Always use a ground plane and place decoupling capacitors nearby to minimize noise, if possible.

# Project Analysis

There were some errors in the board during assembly.

**Hard Errors:**

- No hard errors encountered for this board.

**Soft Errors:**

- Silkscreen marking relatively unused values should help a lot during assembly…
- Due to misassembly, 10k resistors were placed on power indicator LEDs. LED indicators are slightly dimmer (soft error on both 5V and 3.3V LED)
- Capacitors take forever to discharge, since they are discharging 1/10th of design. LDO filter capacitor is discharging at 5mV/sec (which is VERY slow, but keeps the voltage very stable at 3.3V since it can charge quickly).
- Values of resistors should be on a silk screen, since there was space.
- Silkscreen placement could have been better. “No Ground plane” and “Ground Plane” silkscreen are next to test points, not the planes.
- Placing of test points could have been better.

## What went well:

- Soldering of the 1206 parts was relatively easy, since there was enough space between any 2 parts.
- Silkscreen display matches the schematic, and placement of parts are straightforward
- Measurement of signals: test points were properly placed in the schematic, and output of test points are reasonable.

## What didn't go well:

- Lack of focus lead to parts being placed in wrong locations (again)
- Predicting expected signal levels for each test point input: using the oscilloscope took slightly longer time

## Future Improvements:

- Good Test Point placement and Silk Screen placement can help you compare the PCB and schematic much easily. It was enough for this measurement, but would have been much better if test points were aligned.
- Reduce number of different parts, especially resistors and capacitors, as it is easy to misplace them during assembly

## Extra Credit for Report 2:

## Thevenin Resistance of Hex Inverter:

- We can measure Vth with a very high resistance value load (Test Point, since probe/multimeter has high impedance). We can calculate Rth by adding a resistor through the test point and measuring the voltage difference.
- A 47 ohm resistor was placed between test points on the Quiet High test point.


Figure 13: Quiet High Test Point (Left: no resistor, Right: 47 ohm resistor)

- **TP voltage = 5.25V with no resistor, 4.05 with 47 ohm resistor. Rth acts like a voltage divider.**

$$I = \frac{4.05V}{47ohm} = 0.0862A$$
$$R_{th} = \frac{5.25V - 4.05V}{0.0862A} = 13.9ohm$$

- **The Thevenin Resistance of Hex Inverter is 13.9 ohms.**

## LDO configuration w and w/o Filter:

- The resistor next to the capacitor was accidentally assembled with a 10k resistor instead of a 1k resistor, making charge/discharge time very long.
- Oscillations were bigger with the filtering capacitor, likely due to 10k resistors being placed instead of 1k resistors, which likely affected the filter of the system. However, the oscillations are very short and are only 30mVpp and 22mVpp respectively.

Figure 14: LDO 3.3V output oscillation (Left: with 22uF filter capacitor, Right: w/o 22uF filter capacitor)

## Difference between 3.3V and 5V VCC for Hex Inverter:

The hex inverter operates at both 3.3V and 5V (~5.4V measured) rails. Rise time for both 3.3V signal and 5.4V signals were the same at 1.5ns. However, the same rise time for higher voltage rail (5.4V) came at the cost of higher voltage overshoot. From the controls perspective, it is the same, as the overshoot is around 35% of target voltage. So the inverter provides enough slew rate for both 3.3V and 5V rail. Switching noise is much higher due to higher Vcc on 5V rail, due to higher slew rate.

| Vcc | Rise Time | Overshoot | % Overshoot | Quiet Low Vpp | Quiet High Vpp |
|---|---|---|---|---|---|
| 3.25V (LDO) | 1.5ns | 1.17V | 35.9% | 0.56V | 1.22V |
| 5.4V (5V power) | 1.5ns | 1.85V | 34.5% | 1.11V | 2.16V |

Figure 15: Overshoot Results for different Vcc

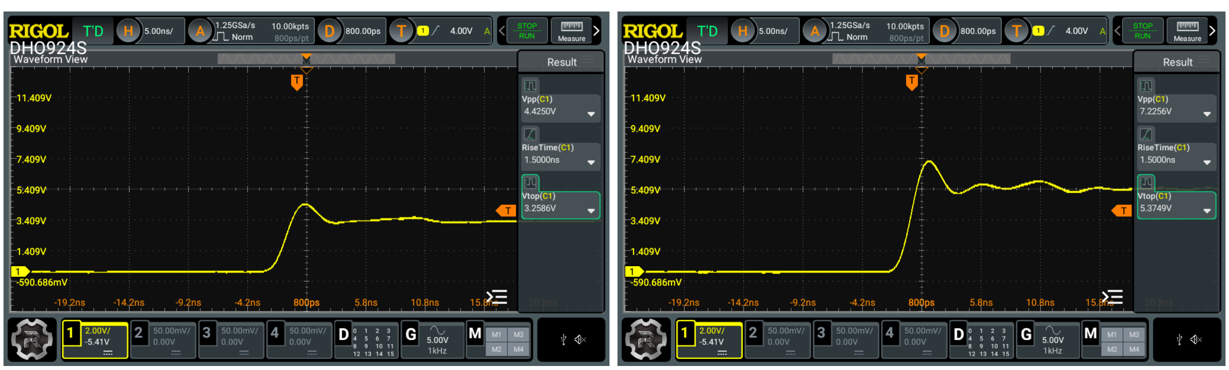

Figure 16: Rise Time of inverter with ground plane (Left: 3.3V, Right: 5V)


Figure 17: Quiet High Switching Noise with ground plane (Left: 3.3V, Right: 5V)