ECEN 5224: Week 5 Lab Report

Simulating Time-Domain Reflections (TDR) with Keysight ADS

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Objective of Lab: Explore effects of time-domain reflections (TDR) on signal integrity, exploring effects of different impedances on source/load.

Summary of Experiment: In this lab, a thevenin voltage source with a pulse was connected to an ideal transmission line and a load (Resistor), with varying source impedance/load impedance. Transient Analysis from Keysight ADS was used to observe voltages over time. Voltage is the most constant when the circuit is electrically short (Rise Time >> Time Delay) or when there is no/little impedance mismatch.

A simple pulse Thevenin Voltage source was modeled with an ideal transmission line (50ohm, 1ns delay) and load resistance. Measuring points were added at the source (after source resistor) and at the load voltage.

Z_source = 3/50/950 ohm, 10-90RiseTime = 0.1ns, Z_load = 50/1meg ohm
Z_tline = 50ohm, TimeDelay = 1ns, V_thevenin = 1V

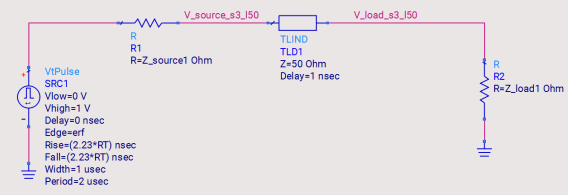

Figure 1: Schematic of TDR Experiment with Thevenin Voltage Source and Load

The reflection coefficient (rho) can be calculated by the formula below. To get no reflection, impedance must be matched between transmission line and the load.

$$\rho = \frac{Z_2 - Z_1}{Z_2 + Z_1}$$

Source resistance at the Voltage Source affects the initial voltage and terminal voltage - 3 Ohm has the highest load voltage, and 950 Ohm with lowest load voltage with 50 Ohm load. However, initial voltage (before it reaches load) is the same regardless of voltage load, since it only “sees” source impedance and transmission line impedance. If source impedance is less than transmission line impedance, overshoots are present in the load. If source impedance is equal to transmission line impedance, there is minimum reflection even when load impedance doesn’t match transmission line impedance. If source impedance is greater than transmission line impedance, there is an undershoot which leads to longer rise times.

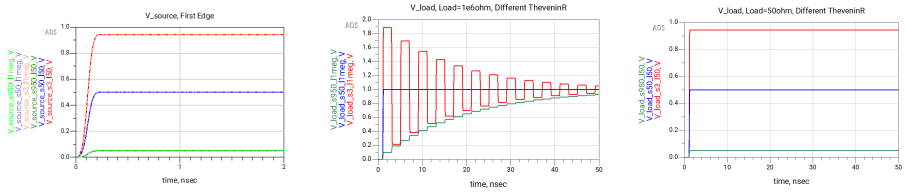

Figure 2: Initial Source Voltage before Time Delay (Left), Load Voltage (Middle: Load=1megaOhm, Right: Load=50Ohm)

Since the transmission line has an impedance of 50 ohms, there are no reflections when load impedance is at 50 ohms. Reflections from 1 megaOhm load makes the load voltage double at the first

peak, since the reflection coefficient is close to 1. There are also reflections on the voltage source, but the amplitude is much lower. On the load voltage, the first peak is double the initial voltage source at the first edge for 1 megaOhm loads. Reflections occur every 2ns (2*TimeDelay) for both on the source and load. In the long run, the voltage drops to its terminal voltage, and the magnitude of reflection decays over time.

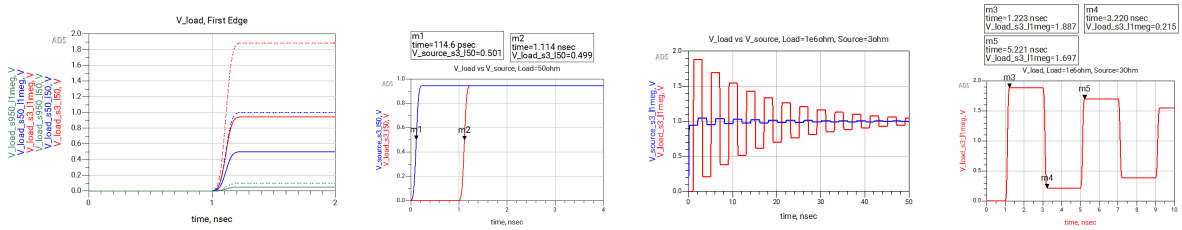

Figure 3: Voltages on V_load and V_source. There is a time delay of 1ns between the voltage source and the load. Reflections occur every 2ns. Reflections on load are much larger than at voltage source. From Left to Right: (First Edge on V_load), (First edge V_source vs. V_load), (Multiple cycles V_source vs V_load)

Reflections occur on source even for 50 ohm loads, if impedance of voltage source is different from the transmission line.

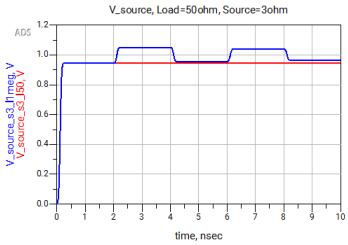

Figure 4: Reflections on Voltage Source for 3 Ohm Source Resistance

Slower rise times do not have an effect on the overshoot (since reflection coefficient is constant), but affects the reflected waveform. However, when the transmission line is electrically short (RT=10ns for 1ns Time Delay), there are minimal or no reflections.

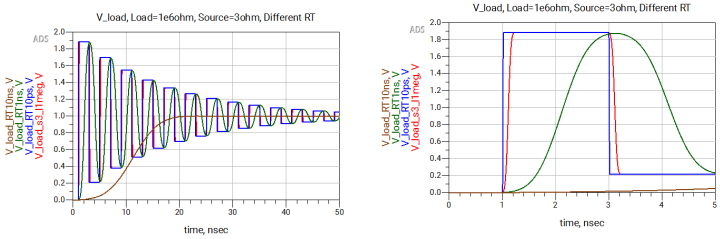

Figure 5: Effects of different Rise Times on signal waveform

Conclusion for Lab: Impedance mismatch between voltage source, transmission lines, and load is the root cause of many signal integrity issues. Whether it be between voltage source and transmission line, or between transmission line and load, there are reflections. When the circuit is electrically long (Rise Time << Time Delay), there is no overshoot. Different rise times affect signal waveforms when electrically short, but not the overshoot. When designing real-life circuits (such as PCB), transmission impedance should be heavily considered to minimize noise. Adding additional source resistors can mitigate the issue, since noise can be reduced if source and transmission line impedances match..